

REMARKS

Reconsideration of the present application is respectfully requested. Claims 1, 3-11 and 17-18 previously presented for examination remain in the application. Claims 1 and 4-8 have been amended and claim 2 has been canceled.

Claims 1-11 stand rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over U.S. Patent No. 5,867,430 to Chen et al. ("Chen") and Applicants' Admitted Prior Art (AAPA), in view of U.S. Patent No. 6,182,189 to Alexis et al. ("Alexis 1").

Claim 2 has been canceled rendering the rejection with respect to that claim moot.

Claim 1 includes the limitations

a memory array having at least a first plane and a second plane, wherein a first partition of the memory array comprises one of the planes and a second partition of the memory array comprises the remaining planes, wherein a write operation is to be performed on the first partition and a read operation is to be concurrently performed on the second partition; and

a status register coupled to the memory array, wherein the status register is to provide status information for at least the first and second planes, the status register being responsive to a memory address associated with one of the first and second partitions to indicate a status of the addressed partition.

(Claim 1)(emphasis added)

Applicants respectfully submit that Chen and Alexis 1, alone or in combination, fail to teach or suggest the limitations of claim 1 including at least the status register that provides status information for at least two planes responsive to an address.

It is admitted in the Office Action that Chen fails to teach such a status register. While Alexis 1 mentions that a single status register may be used, Alexis 1 fails to teach or suggest a status register that is responsive to an address in the claimed manner to provide status information for multiple planes. Thus, the combination of Chen and Alexis 1 would also fail to teach or suggest the claimed features of applicants' invention.

For at least this reason, claim 1 is patentably distinguished over Chen and Alexis 1, alone or in combination.

Independent claim 6 includes a limitation similar to that argued above in reference to claim 1. Claims 3-5 and claims 7-11 depend from and further limit claims 1 and 6, respectively, and, thus, for similar reasons should also be found to be distinguished over Chen and Alexis 1, alone or in combination.

Claims 18-19 stand rejected under 35 U.S.C. § 103(a) as being considered to be unpatentable over Chen in view of U.S. Patent No. 6,260,103 to Alexis et al. ("Alexis 2").

Claim 18 includes the limitations

means for partitioning a memory array into a fixed first partition and a variable second partition to enable multiple operations to be performed on the memory array at the same time;
and

means for monitoring the operations performed on the memory array.

(Claim 18)(Emphasis added)

Applicants respectfully submit that, because Alexis 2 and the present invention have a common assignee, and the Alexis 2 patent issued after the filing

date of the present invention, under 35 U.S.C. § 103(c), Alexis 2 may be used as a reference to preclude patentability of the present invention.

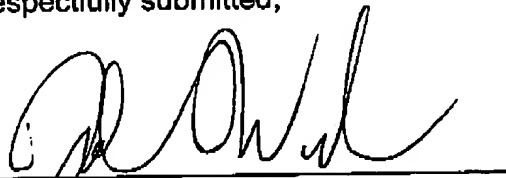
Further, as admitted by the Examiner in paragraph 5 of the Office Action, Chen does not specifically teach that the second partition is variable. For at least these reasons, claim 18 is patentably distinguished over the cited references.

Claim 19 depends from and further limits claim 18 and thus, should be found to be allowable for at least the same reasons.

Based on the foregoing, applicants respectfully submit that the applicable objections and rejections have been overcome, and claims 1-11 and 18-19 are in condition for allowance. If the examiner disagrees or believes that further discussion will expedite prosecution of this case, the examiner is invited to telephone applicants' representative at the number indicated below.

If there are any charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,



John Patrick Ward
Reg. No. 40,216

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BLAKELY, SOKOLOFF, TAYLOR & ZAFMAN LLP
12400 Wilshire Boulevard
Seventh Floor
Los Angeles, CA 90025-1030
(408) 720-8300